IN THE CLAIMS:

Amend claims 1 and 8 to read as follows (the attached appendix sets forth the amended claims with markings showing the differences between the original text and the text as hereby amended):

1. (Twice amended) A method for forming metal salicide regions and metal salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

(a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

(b) depositing a metal layer on the IC structure in a controlled manner;

(c) forming a photoresist masking layer on portions of the MOS transistor structures where metal salicide regions are to be formed;

(d) removing the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed;

(e) after step (d), stripping the photoresist masking layer; and

(f) after step (e), reacting metal in the metal layer with silicon in the exposed silicon surfaces to form metal salicide regions, wherein

step (b) includes the step of controlling at least one metal deposition parameter such that the metal layer has at least one predetermined property that causes the reaction of the metal with the silicon during step (f) to occur in a source limited manner and limits metal salicide crawl during step (f) beyond at least one of the portions of the MOS transistor structures where metal salicide regions are to be formed.

8. (Twice amended) A method for forming cobalt salicide regions and cobalt salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

(a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

(b) depositing a cobalt layer on the IC structure in a controlled manner;

(c) depositing a capping layer on the cobalt layer;